

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte URI ELZUR, FRANKIE FAN, STEVEN B. LINDSAY,
and SCOTT S. MCDANIEL

Appeal 2007-0457
Application 10/652,267
Technology Center 2100

Decided: April 23, 2007

Before JOSEPH F. RUGGIERO, LANCE LEONARD BARRY, and
JEAN R. HOMERE, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1 through 33. We have jurisdiction under 35 U.S.C. § 6(b) to decide this appeal.

Appellants invented a method and system for offloading Transport Control Protocol (TCP) processing between a host and a network interface card (NIC). Particularly, a TCP enabled Ethernet controller (TEEC) processes an incoming packet without reassembly, and temporarily buffers the packet in an internal elastic buffer before forwarding the packet to the host computer. (Specification 11).

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A system for offloading TCP processing, the system comprising:

a host;

a network interface card (NIC) coupled to said host, said NIC comprising, a TCP enabled Ethernet controller (TEEC), said TEEC comprising, at least one internal elastic buffer, wherein said TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, said processing occurring without reassembly.

In rejecting the claims on appeal, the Examiner relied upon the following prior art:

Boucher(1)	US 6,427,173 B1	Jul. 30, 2002
Susnow	US 6,751,235 B1	Jun. 15, 2004
		(filed Jun. 27, 2000)
Boucher(2)	US 6,757,746 B2	Jun. 29, 2004
		(filed Feb. 20, 2001)

The Examiner rejected the claims on appeal as follows:

- A. Claims 1 through 5 and 7 through 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Boucher(2).¹
- B. Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Boucher(2).

Appellants contend² that Boucher does not anticipate claims 1 through 5 and 7 through 33. Particularly, Appellants contend that Boucher does not fairly teach or suggest a TEEC that processes an incoming packet without reassembly, and that temporarily buffers the packet in an internal elastic buffer. (Br. 8 and 13; Reply Br. 4 and 7). The Examiner, in contrast, contends that Boucher teaches the limitations of representative claim 1 as a NIC card for processing incoming packets, and as a data synchronization buffer for buffering the packets. (Answer 8). The Examiner therefore concludes that Boucher anticipates representative claim 1. Appellants further contend that Boucher does not render claim 6 unpatentable since it does not teach that the NIC uses only the elastic buffer to temporarily store the packet. (Br. 25-26). In response, the Examiner contends that using only an elastic buffer to temporarily store packets, as recited in dependent claim 6, is well-known in the art. Therefore, the Examiner concludes that it would

¹ Boucher(2) incorporates by reference the complete disclosure of Boucher (1). See column 1, lines 34-44.

² This decision considers only those arguments that Appellants submitted in the Appeal and Reply Briefs. Arguments that Appellants could have made but chose not to make in the Briefs are deemed to have been waived. See 37 C.F.R. § 41.37(c)(1) (vii)(eff. Sept. 13, 2004). See also *In re Watts*, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

have been obvious to modify Boucher's teaching by using only an elastic buffer to temporarily store the data. (Answer 6).

We reverse.

ISSUES

The *pivotal* issues in the appeal before us are as follows:

- (1) Have Appellants shown that the Examiner has failed to establish that Boucher anticipate the claimed invention under 35 U.S.C. § 102(e), when Boucher teaches synchronizing/assembling incoming packet frames within an ASIC chip, and transferring the frames to an external buffer, and subsequently transferring the packet data to a host?
- (2) Have Appellants shown that the Examiner has failed to establish that one of ordinary skill in the art, at the time of the present invention, would have found that the disclosure of Boucher renders the claimed invention unpatentable under 35 U.S.C. § 103(a)?

FINDINGS OF FACT

The following findings of fact are supported by a preponderance of the evidence.

The invention

1. Appellants invented a method and system for offloading TCP processing between a host memory (230) and a network interface card (NIC) (250). (Specification 13).

2. As depicted in figure 2, the NIC (250) includes a TCP enabled Ethernet controller (TEEC) (270), which in turn includes a Tx elastic buffer³ (280) and an Rx elastic buffer (290) for respectively storing outgoing and incoming packets. (Specification 14).
3. Upon receiving a packet from the Ethernet (260), TEEC processes the incoming packet without reassembly, and temporarily buffers the packet in the internal elastic buffer (290) before forwarding the packet to the host interface (240). (Specification 14).
4. The host memory subsequently receives the dispatched packet via the memory controller (220). (Specification 14).

The Prior Art Relied upon

5. Boucher(2) discloses a network interface device (102) that includes a register (112), a buffer (2114) and a DMA engine for directly writing a multi-packet message into the memory of a computer host (100) without TPC or IP headers. (Col. 5, ll. 40-62).
6. Boucher(1) discloses a system for accelerated data transfer and offloading between a host computer (20) and an intelligent network interface card (INIC) (200). (Col. 24, ll. 60-67).
7. As depicted in figure 21, the INIC (200) includes an ASIC chip (400), a DRAM (460) and a buffer (2114). (Col. 24, l. 61- col. 25, l. 5).

³ Appellants' Specification defines an elastic buffer as a small (e.g. 64 KB) on chip packet buffer utilized to provide elasticity. (Specification 11, paragraph 39).

8. The ASIC chip, in turn, includes transmit sequencers TXSEQ (2104) and RXSEQ (2105) for respectively handling outgoing and incoming data packets. (Col. 25, ll. 9-10).
9. Further, as depicted in figure 22, the receive sequencer RXSEQ (2105) synchronizes and assembles incoming packet data before the packet is transferred to the host. (Col. 25, ll. 17-27).
10. Particularly, the RXSEQ (2105) uses a packet synchronization sequencer (2201) for instructing the data synchronization buffer⁴ (2200) to load a receive byte. (Col. 25, ll. 17-27).
11. Then, it uses a packet processing sequencer (2204) to determine data availability in the sync buffer (2200) and subsequently uses a packet processing sequencer (2204) to instruct the data assembly register (2202) to load a byte of data from sync buffer (2200). (Col. 26, l. 61- col. 27, l. 35).
12. RXSEQ then transfers the synchronized packet data from its internal buffer (2217) to an external buffer (2114) in the DRAM (460). (Col. 27, ll. 36-38).
13. After all packet data has been transferred to buffer 2114, the packet processing sequencer (2204) creates a summary (2224) indicating whether the packet should be put on a fast path or a slow path for transfer to the host. (Col. 29, ll. 6-19).

⁴ The data synchronization buffer is four bytes deep. (Col. 26, ll. 64-65). Therefore, it qualifies as an elastic buffer (i.e. not a multi-megabyte memory that is utilized for packet reordering reassembly or retransmission, as defined in Appellants' Specification, 11).

PRINCIPLES OF LAW

1. ANTICIPATION

It is axiomatic that anticipation of a claim under § 102 can be found if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76, 77 USPQ2d 1321, 1325-26 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue “reads on” a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346, 51 USPQ2d 1943, 1945 (Fed Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (internal citations omitted).

2. OBVIOUSNESS

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir.

1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. *Oetiker*, 977 F.2d at 1445, 24 USPQ2d at 1444. *See also Piasecki*, 745 F.2d at 1472, 223 USPQ at 788. Thus, the Examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the Examiner's conclusion.

ANALYSIS

35 U.S.C. § 102(e) REJECTION

As set forth above, representative claim 1 requires temporarily storing an incoming packet in an internal elastic buffer and processing the packet without reassembly. As detailed in the findings of fact section above, we have found that Boucher (1 and 2) discloses an ASIC 400 chip for processing incoming data packets. (Findings of fact 7 and 8). We have found, however, that Boucher's processing of the data packets in the ASIC chip involves (1) synchronizing the received packet data; (2) assembling the frames of the packet; and then (3) transferring the synchronized/assembled packet data to an external buffer. (Finding of facts 9 through 14). In light of these findings, it is our view that Boucher does not teach processing an incoming packet without reassembly.

Further, we have found that Boucher's external buffer holds each received piece of packet data until it receives all data pertaining to the packet

before it transfers the received packet data to the host. (Finding of fact 13). Additionally, we have found no evidence that the external buffer where the packet data is being held is an elastic buffer. We agree with the Examiner that Boucher's data synchronization buffer is an elastic buffer that is internal to the ASIC. (Finding of fact 10). We note, however, the data synchronization buffer is not being used for temporarily storing portion of a TCP IP packet. Rather, it is being used for the purpose of storing packet synchronization data. (Findings of fact 10 and 11). In light of these findings, it is our view that Boucher does not teach an internal elastic buffer for temporarily storing incoming packet data. It follows that the Examiner erred in rejecting representative claim 1 as being anticipated by Boucher. It follows for the same reasons that the Examiner erred in rejecting claims 2 through 5 and 7 through 33 as being anticipated by Boucher.

35 U.S.C. § 103(a) REJECTION

Now, we turn to the rejection of dependent claim 6 as being unpatentable over Boucher. We note that claim 6 depends directly from claim 1. Thus, claim 6 also requires temporarily storing an incoming packet in an internal elastic buffer and processing the packet without reassembly. For the reasons set forth in the discussion of representative claim 1 in the preceding paragraph, we find that Boucher does not at least teach the limitations of claim 6, as noted above. We therefore conclude that Boucher does not render claim 6 unpatentable.

CONCLUSION OF LAW

On the record before us, Appellants have shown that the Examiner has failed to establish that Boucher anticipates the claimed invention under 35 U.S.C. § 102(e). Further, Appellants have shown that the Examiner has failed to establish that one of ordinary skill in the art at the time of the present invention, would have concluded that Boucher renders the claimed invention unpatentable under 35 U.S.C. § 103(a).

DECISION

We reverse the Examiner's decision to reject claims 1 through 5 and 7 through 33 under 35 U.S.C. § 102(e) as being anticipated by Boucher. We also reverse the Examiner's decision to reject claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Boucher.

REVERSED

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